CNF formuals of parameterized width

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Abstract. In this document, we describe a parameterized class of of unsatisfiable formulas $F(r, m)$. These formulas specify equivalence checking of circuits of a simple structure (a cascade of blocks). Formulas $F(r, m)$ are meant for studying how the formula width (controlled by parameter r) and "amount of structure" (controlled by parameter m) influence the performance of a SAT-solver.

1 Formulas $F(r, m)$

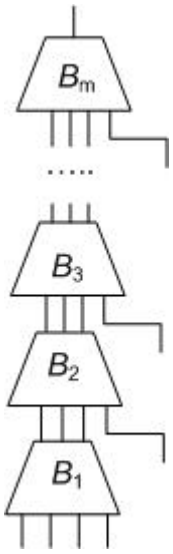

Fig. 1. High-level structure of circuit $N(3, m)$

Formula $F(r, m)$ describes equivalence checking of two circuits $N(r, m)$ and $N'(r, m)$. Both circuits have the same high-level structure shown in Figure 1 for $N(3, m)$. Circuit $N(r, m)$ is a cascade of m combinational blocks B_i. The first $m - 1$ blocks B_i have $r + 1$ inputs and r outputs. The last block B_m has $r+1$ inputs and only one output that is also the output of N. All the inputs of the block B_1 are also the primary inputs of circuit N. One input of each block B_i, $i = 2 \ldots, m$ is also the primary input of circuit N. The other r inputs of B_i are fed by the outputs of the previous block B_{i-1}.

Formula $F(r, m)$ specifies the so-called miter of circuits $N(r, m)$ and $N'(r, m)$. The miter of N and N' is a circuit that evaluates to 1 if and only if N and N' are functionally inequivalent. An example of a miter is shown in Figure 2. The inputs of N and N' are shared and their outputs feed an XOR gate. The miter evaluates to 1 if and only for some input assignment N and N' produce different outputs and so inequivalent. Formula $F(r, m)$ is equal to $H_{N(r,m)} \wedge H_{N'(r,m)} \wedge H_G \wedge z$. Here, CNF formulas $H_{N(r,m)}$ and $H_{N'(r,m)}$ specify the functionality of circuits N and N' respectively. (These formulas are obtained from N and N' using regular Tseitsin's

transformations.) The formula H_G specifies the XOR gate G of the miter and the unit clause z forces to set the output of the gate G (specified by variable z) to 1.

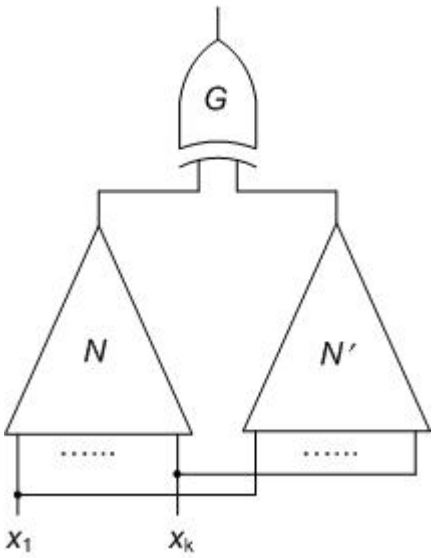

Fig. 2. Miter of circuits N and N'