Curriculum Vitae

Eugene (Evgueni) Goldberg

Contact Information

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Personal Details

Place of birth: Minsk, Belarus
Present Citizenship: US

Goal

An R&D position where I can apply my rich experience in hardware/software verification and/or hardware logic design and synthesis

Education

1995:
PhD defense, Institute of Technical Cybernetics of the Belorussian Academy of Sciences. PhD thesis "Methods of optimal PLA implementation of digital devices specified by multiple-valued functions".

1988 - 1991:
PhD student at the Institute of Technical Cybernetics of the Belorussian Academy of Sciences, branch "Control in technical systems".

1977 - 1983:
BS, MS in theoretical physics, Belorussian State University

Work Experience

2016 - till now: *Consultant at DiffBlue, Oxford, UK*

July 2013 - 2015: *Research Assistant Professor at Northeastern University, College of Computer and Information Science*

August 2009 - July 2013: *Researcher at the same location*

I started at NEU by working on a project funded by SRC (Semiconductor Research Corporation) called "Decision procedures for system-level verification". Later I got awarded an SRC grant funded also by IBM called "Efficient bit-level solvers for quantified formulas". Besides, I got awarded two NSF grants for the projects called "Generation of high-quality tests by treating

tests as proof encoding" and "Dynamic abstractions for verification". Some results of my work on these four projects are described below.

November 1997 - November 2008: *Research Scientist at Cadence Berkeley Labs (now Cadence Research Labs)*

My main interests were the creation of efficient algorithms for computationally hard problems in the areas of logic synthesis, test and verification (some highlights of my results are shown below). Algorithms I developed have been used in logic synthesis and formal verification tools of Cadence

May 1996 - November 1997: *Postdoc Research at the University of California at Berkeley (hosted by prof. Robert Brayton)*

I developed new algorithms for two-level logic minimization and state encoding. I also worked on developing a new type of Binary Decision Diagrams (data structure for logic manipulation) and new search pruning techniques in discrete optimization (in particular, for the covering problem)

Dec 1986 - May 1996: *Researcher at the Laboratory of Logic Design of Integrated Circuits at the Belorussian Academy of Sciences*

I developed various algorithms for synthesis and testing of digital circuits, including a few VLSI CAD systems used by the local industry

Sept 1983 - Dec 1986: *Researcher at the Laboratory of Automation of Scientific Research at the Belorussian Academy of Sciences*

Designing and developing software for the oil distribution control system of the main oil storage facility of Minsk

Some highlights of my research

SAT-Solving:

I co-authored BerkMin (DATE-2002) and Forklift, award-winning SAT-solvers (SAT-2002, SAT-2003 competitions). To verify resolution proofs generated by a SAT-solver, I have co-developed the concept of clause proofs (DATE-2003). Currently, clause proofs is a de-facto standard in proof verification.

Multi-Property Checking:

I have co-developed a new approach to multi-property verification based on the notion of local proofs (DATE-2018). This approach avoids costly generation of long counterexamples by identifying a small subset of failing properties responsible for all other failures.

Test Generation:

I have developed methods for generating high-quality tests off a resolution proof (VMCAI-2008) and off a projection of an unsatisfiable formula onto a small set of variables (FMCAD-2018). These methods are based on the machinery of stable sets of points (CADE-2002).

Equivalence Checking:
I co-developed a method for equivalence checking where a SAT-solver was used to identify functionally equivalent cut points (DATE-2001). (At the time, such identification was done by BDDs.) I have also developed a new approach to exploiting the similarity of circuits to be checked for equivalence (FMCAD-2016). In contrast to the existing methods, this approach is complete. For instance, it can be applied if the circuits to be compared are structurally similar but do not have any functionally equivalent internal points.

Redundancy Based Reasoning:
I have co-developed redundancy based reasoning, a new approach to solving CNF formulas with quantifiers (FMCAD-12, FMCAD-13). A major problem here is that one has to efficiently enumerate the subspaces where the formula at hand is satisfiable. Redundancy based reasoning allows to solve a formula with quantifiers without deciding if this formula is satisfiable in the current subspace.

Partial Quantifier Elimination:
I have co-developed partial quantifier elimination, a new approach to solving verification problems (HVC-14). In contrast to complete quantifier elimination, in partial quantifier elimination, only a small part of the formula is taken out of the scope of quantifiers. The appeal of partial quantifier elimination is that a) it provides a language for incremental computing and b) it is dramatically more efficient than complete quantifier elimination. Many verification problems e.g. equivalence checking (FMCAD-16) can be solved by partial quantifier elimination.

Awards

- E. Goldberg, M. Güdemann, D. Kroening, R. Mukherjee. Efficient verification of multi-property designs (the benefit of wrong assumptions), *Best paper award* at DATE-2018, Dresden, pp. 43-48.
- E.Goldberg, M.Prasad, R.Brayton. Using Problem Symmetry in Search Based Satisfiability Algorithms, *Best paper award* at DATE-2002, Paris,pp. 134-141.
- E. Goldberg and Y. Novikov. BerkMin: A Fast and Robust Sat-Solver. DATE 2002, Design, Automation, and Test in Europe. *The Most Influential Papers of 10 Years DATE*, R. Lauwereins and J. Madsen (Eds.) 2008, 516 p. According to Google-scholar, the *citation count* of this paper is 1066.
- The SAT-solver BerkMin I co-authored with Yakov Novikov became the *SAT-2002 competition winner* in the category of satisfiable handmade benchmarks.
- The SAT-solver Forklift (an advanced version of BerkMin) I co-authored with Yakov Novikov became the *SAT-2003 competition winner* in the categories of "only satisfiable" and "both satisfiable and unsatisfiable" industrial benchmarks.

- *Cadence Labs Award* for Distinguished Contributions to Research and Technology Transfer (December 2003).

Invited Talks

- A new method of checking Satisfiability in Propositional Logic, Dagstuhl seminar: Computer Aided Design and Test: BDDs vs. SAT, Dagstuhl, Germany, 28 Jan.- 2 Feb. 2001.
- Three lectures on "Practical algorithms for the SAT-Problem" given at Humboldt University, Berlin, October 27-29, 2006.
- Boundary point elimination: a path to structure-aware SAT-solvers. Dagstuhl seminar: Algorithms and Applications for Next Generation SAT Solvers, Dagstuhl, Germany, Nov.8-13, 2009.

Patents

- US Patent 7,356,519 - Method and system for solving satisfiability problems (with Yakov Novikov)
- US Patent 7,380,226 - Systems, methods, and apparatus to perform logic synthesis preserving high-level specification
- US Patent 7,600,211 - Toggle equivalence preserving logic synthesis (with Kanupriya Gulati).
- US Patent 7,610,570 - Method and Mechanism for using systematic local search for SAT solving.
- US Patent 7,853,903 - Method and mechanism for performing simulation off resolution proof (with Felice Balarin)
- US Patent 7,992,113 - Method and apparatus for decision making in resolution based SAT-solvers.
- US Patent 8,438,513 - Quantifier elimination by dependency sequents (with Pete Manolios)

Some publications

(Can be downloaded from www.eigold.tripod.com/papers.html)

Conferences papers

- E. Goldberg. *Complete Test Sets And Their Approximations*, FMCAD-18, Austin, pp. 31-38.
- E. Goldberg, M. Güdemann, D. Kroening, R. Mukherjee. *Efficient verification of multi-property designs (the benefit of wrong assumptions)*, DATE-2018, Dresden, pp. 43-48.

- E.Goldberg. *Equivalence checking by logic relaxation*, Proceedings of FMCAD-16, pp. 49-57.
- E.Goldberg, P.Manolios. *Partial Quantifier Elimination*, HVC-14, Israel, LNCS 8855, pp.148-165, 2014.
- E.Goldberg, P.Manolios.*Quantifier Elimination Via Clause Redundancy*, FMCAD-13, Portland, OR, USA.
- E.Goldberg, P.Manolios. *Quantifier Elimination by Dependency Sequents*, FMCAD-12, pp. 34-44, Cambridge, UK.
- E.Goldberg, P.Manolios. *Generating High-Quality Tests for Boolean Circuits by Treating Tests as Proof Encoding*, TAP-2010, Malaga, Spain, LNCS 6143, pp.101-116.
- E.Goldberg *Boundary points and resolution*, SAT-2009, Swansea,Wales,UK, LNCS 5584, pp.147-160.
- E.Goldberg. *On bridging simulation and formal verification*, VMCAI-2008, San Francisco, USA, LNCS 4905, pp.127-141.
- E.Goldberg. *A decision-making procedure for resolution-based SAT-solvers*, SAT-2008, Guangzhou, China, LNCS 4996,pp. 119-132.
- E.Goldberg. *On Equivalence Checking and Logic Synthesis of Circuits with a Common Specification*, Proceedings of GLSVLSI, Chicago, April 17-19, 2005,pp.102-107.
- E.Goldberg. *Equivalence Checking of Circuits with Parameterized Specifications*, SAT-2005. Lecture Notes in Computer Science, vol. 3569, p. 107.
- E. Goldberg. *Testing Satisfiability of CNF Formulas by Computing a Stable Set of Points*, Proceedings of Conference on Automated Deduction, CADE 2002,LNCS, vol. 2392,pp.161-180.
- E.Goldberg, Y.Novikov. *Verification of proofs of unsatisfiability for CNF formulas*, DATE-2003, Munich, pp.886-891.
- E.Goldberg, M.Prasad, R.Brayton. *Using Problem Symmetry in Search Based Satisfiability Algorithms*, DATE-2002, Paris,pp. 134-141.
- E.Goldberg, Y. Novikov. *BerkMin: A Fast and Robust SAT-solver*, DATE-2002, Paris, pp.142-149.
- E. Goldberg, M. Prasad, R. Brayton. *Using SAT for combinational equivalence checking*, DATE-2001, pp. 114 -121.
- E. Goldberg , A.Saldanha. *Timing analysis with implicitly specified false paths*, VLSI Design 2000. Calcutta India, Pages 518 -522 .
- E. Goldberg, T. Villa, R. Brayton, A. Sangiovanni-Vincentelli, A.L. *A fast and robust exact algorithm for face embedding*, ICCAD-97. Los Alamitos, CA, USA, IEEE Comput. Soc, 1997. p. 296-303.

- E. Goldberg, L. Carloni, T. Villa, R. Brayton. *Negative thinking by incremental problem solving: application to unate covering*, ICCAD-97, Los Alamitos, CA, USA: IEEE Comput. Soc, 1997, pp. 91-99.

Journals

- E.Goldberg. *A Resolution Based SAT-solver Operating on Complete Assignments*, Journal on Satisfiability, Boolean Modeling and Computation, Vol. 5 (2008), pp. 217-242.
- E.Goldberg. *Testing Satisfiability of CNF Formulas by Computing a Stable Set of Points*, Annals of Mathematics and Artificial Intelligence, 43 (1-4): 65- 89, Jan. 2005.
- E.Goldberg. *Proving Unsatisfiability of CNFs locally*, Journal of Automated Reasoning. vol 28:417-434, 2002.
- ⋆ E.Goldberg, L.Carloni, T. Villa, R. Brayton, A. Sangiovanni-Vincentelli. *Negative Thinking in Branch-and-Bound: the Case of Unate Covering*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 19, No. 3, March 2000.
- ⋆ E.Goldberg,T.Villa,R.Brayton,A.Sangiovanni-Vincentelli. *Theory and algorithms for Face Hypercube Embedding*, IEEE trans. on CAD. Vol. 17, 6,1998, pp.472-488.

Books

- E.Goldberg. *What Sat-solvers can and cannot do. A chapter in Advanced Formal Verification*, pp.1-43. Kluwer Academic Publishers, edited by Rolf Drechsler, 2004, 624 p.
- E.Goldberg, P.Manolios. *Boundary points and resolution*, in Advanced Techniques in Logic Synthesis, Optimizations and Applications, Sunil P. Khatri and Kanupriya Gulati, editors, Springer, 2010, chapter 7, pp. 109-128.

References

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