

On Verifying Designs With Incomplete Specification

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Abstract—Incompleteness of a specification *Spec* creates two problems. First, an implementation *Impl* of *Spec* may have some *unwanted* properties that *Spec* does not forbid. Second, *Impl* may break some *desired* properties that are not in *Spec*. In either case, *Spec* fails to expose bugs of *Impl*. In an earlier paper, we addressed the first problem above by a technique called Partial Quantifier Elimination (PQE). In contrast to complete QE, in PQE, one takes out of the scope of quantifiers only a small piece of the formula. We used PQE to generate properties of *Impl* i.e. those *consistent* with *Impl*. Generation of an unwanted property means that *Impl* is buggy. In this paper, we address the second problem above by using PQE to generate false properties i.e. those that are *inconsistent* with *Impl*. Such properties are meant to imitate the missing properties of *Spec* that are not satisfied by *Impl* (if any). A false property is generated by modifying a piece of a quantified formula describing ‘the truth table’ of *Impl* and taking this piece out of the scope of quantifiers. By modifying different pieces of this formula one can generate a “structurally complete” set of false properties. By generating tests detecting false properties of *Impl* one produces a high quality test set. We apply our approach to verification of combinational and sequential circuits.

I. INTRODUCTION

One of the drawbacks of formal verification is that the set of properties describing a design usually does not specify the latter completely. Incompleteness of a specification *Spec* creates two problems. First, an implementation *Impl* of *Spec* may have some *unwanted* properties that *Spec* does not forbid. Second, *Impl* may break some *desired* properties that are not in *Spec*. In either case, *Spec* fails to expose bugs of *Impl*. In testing, the incompleteness of verification is addressed by using a set of tests that is complete *structurally* rather than functionally. Structural completeness is achieved by probing every piece of the design under test.

In [5], we used the idea of structural completeness to attack the first problem above. The idea was to use a technique called partial quantifier elimination (PQE) to generation properties *consistent* with *Impl*. In contrast to complete quantifier elimination, PQE takes out of the scope of quantifiers only a small piece of formula. A property $Q(V)$ of *Impl* is produced by applying PQE to formula $\exists W[F(V, W)]$ defining “the truth table” of *Impl*. Here F describes the functionality of *Impl* and V, W are sets of external and internal variables of *Impl* respectively. If Q is not implied by *Spec*, then the latter is incomplete. If Q describes an unwanted property of *Impl*, the latter is buggy. Otherwise, a new property is added to *Spec* to make it imply Q . By taking different pieces of F out of the scope of quantifiers, one can build a specification that is *structurally complete*.

In this paper, we continue this line of research by addressing the second problem above. Namely, we use PQE to generate

false properties i.e. those *inconsistent* with *Impl*. They are meant to imitate the missing properties of *Spec* not satisfied by *Impl* (if any). Tests breaking a false property may expose a bug that was not discovered due to *Spec*’s lacking a property not satisfied by *Impl*. A false property $Q(V)$ is generated in two steps. First, a new formula F^* is obtained from F by a slight modification. Then the modified part is taken out of the scope quantifiers from $\exists W[F^*]$. If F^{**} and F are not logically equivalent, this produces a property Q that is implied by F^* but not by F . By modifying different parts of F one can generate a “structurally complete” set of false properties. By generating tests breaking these properties one can build a high quality test.

Our contribution is as follows. First, we show that one can use PQE to generate false properties of *Impl* for combinational circuits. Second, we describe an algorithm that, given a combinational circuit, forms a structurally complete set of false properties of this circuit. Third, we extend our approach to sequential circuits. Fourth, to show the high quality of tests generated off false properties we relate the former to tests detecting stuck-at faults.

The main body¹ of this paper is structured as follows. Basic definitions are given in Section II. In Section III, we describe generation of false properties for combinational circuits. A procedure for building a structurally-complete set of false properties is given in Section IV. Section V extends our approach to sequential circuits by showing how one can generate false safety properties. We relate our approach to fault/mutation detection in Section VI. Finally, we make some conclusions in Section VII.

II. BASIC DEFINITIONS

In this paper, we consider only propositional formulas. We assume that every formula is in conjunctive normal form (CNF). A *clause* is a disjunction of literals (where a literal of a Boolean variable w is either w itself or its negation \bar{w}). So a CNF formula H is a conjunction of clauses: $C_1 \wedge \dots \wedge C_k$. We also consider H as the *set of clauses* $\{C_1, \dots, C_k\}$.

Definition 1: Let V be a set of variables. An **assignment** \vec{q} to V is a mapping $V \rightarrow \{0, 1\}$.

Definition 2: Let H be a formula. $\text{Vars}(H)$ denotes the set of variables of H .

Definition 3: Let $H(V, W)$ be a formula where V, W are sets of variables. The **Quantifier Elimination (QE)** problem specified by $\exists V[H]$ is to find formula $H^*(W)$ such that $H^* \equiv \exists V[H]$.

¹Some additional information is given in the appendix.

Definition 4: Let $H_1(V, W)$, $H_2(V, W)$ be formulas where V, W are sets of variables. The **Partial QE (PQE)** problem of taking H_1 out of the scope of quantifiers in $\exists V[H_1 \wedge H_2]$ is to find formula $H_1^*(W)$ such that $\exists V[H_1 \wedge H_2] \equiv H_1^* \wedge \exists X[H_2]$. Formula H_1^* is called a **solution** to PQE.

Remark 1: Note that if H_1^* is a solution to the PQE problem above and a clause $C \in H_1^*$ is implied by H_2 alone, then $H_1^* \setminus \{C\}$ is a solution too. So if all clauses of H_1^* are implied by H_2 , then an empty set of clauses is a solution too (in this case, $H_1^* \equiv 1$).

Let $N(X, Y, Z)$ be a combinational circuit where X, Y, Z are sets of input, internal and output variables respectively. Let N consist of gates g_1, \dots, g_m . A formula $F(X, Y, Z)$ specifying the functionality of N can be built as $G_1 \wedge \dots \wedge G_m$ where $G_i, 1 \leq i \leq m$ is a formula specifying gate g_i . Formula G_i is constructed as a conjunction of clauses falsified by the incorrect combinations of values assigned to G_i . Then every assignment satisfying G_i corresponds to a consistent assignment of values to g_i and vice versa.

Example 1: Let g be a 2-input AND gate specified by $v_3 = v_1 \wedge v_2$. Then formula G is constructed as $C_1 \wedge C_2 \wedge C_3$ where $C_1 = v_1 \vee \bar{v}_3$, $C_2 = v_2 \vee \bar{v}_3$, $C_3 = \bar{v}_1 \vee \bar{v}_2 \vee v_3$. Here, the clause C_1 , for instance, is falsified by assignment $v_1 = 0, v_2 = 1, v_3 = 1$ inconsistent with the truth table of g .

III. GENERATION OF FALSE PROPERTIES

In this section, we describe generation of false properties of a combination circuit by PQE. Subsection III-A explains our motivation for building false properties. Subsection III-B presents construction of false properties by PQE. In Subsection III-C, we describe generation of tests breaking these properties and argue that these tests are of very high quality.

A. Motivation for building false properties

Let $\mathcal{P} = \{P_1(X, Z), \dots, P_k(X, Z)\}$ be a specification of a combinational circuit. Here $P_i, i = 1, \dots, k$ are properties² of this circuit and X and Z are the sets of input and output variables respectively. Let $N(X, Y, Z)$ be an implementation of the specification \mathcal{P} where Y is the set of internal variables. Let $F(X, Y, Z)$ be a formula describing N (see Section II). Assume that N satisfies all properties of \mathcal{P} i.e. $F \Rightarrow P_i, i = 1, \dots, k$.

The specification \mathcal{P} is complete if it fully defines the input/output behavior of N i.e. if $P_1 \wedge \dots \wedge P_k \Rightarrow \exists Y[F]$. Suppose that \mathcal{P} is *incomplete*. As we mentioned in the introduction, this may lead to overlooking buggy input/output behaviors of N . In this paper, we address this problem by generating false properties of N . The latter are meant to imitate properties absent from \mathcal{P} that N does not satisfy. The idea here is that tests breaking these false properties may expose the buggy behaviors mentioned above.

²The fact that P_i is a property means that an implementation satisfying P_i cannot output \bar{z} for an input \bar{x} if $P_i(\bar{x}, \bar{z}) = 0$.

B. Building false properties by PQE

Let $F^*(X, Y, Z)$ be a formula obtained from F by replacing a set of clauses G with those of G^* . Let $F' = F \setminus G$. (So, $F = G \wedge F'$.) Then the formula F^* equals $G^* \wedge F'$. Let $T_{tbl}(X, Z)$ and $T_{tbl}^*(X, Z)$ denote the “truth tables” of F and F^* respectively. That is $T_{tbl} = \exists Y[F]$ and $T_{tbl}^*(X, Z) = \exists Y[F^*]$. An informal requirement to G^* is that it is unlikely to be implied by F . (Otherwise, the technique we describe below cannot produce a false property.) One more requirement³ to G^* is that for every assignment \bar{x} there exists \bar{z} such that $T_{tbl}^*(\bar{x}, \bar{z}) = 1$. (This is trivially true for $T_{tbl}(X, Z)$ because the latter is derived from F specifying a *circuit*.)

Let $Q(X, Z)$ be a solution to the PQE problem of taking G^* out of the scope of quantifiers in $\exists Y[G^* \wedge F']$. That is $\exists Y[G^* \wedge F'] \equiv Q \wedge \exists Y[F']$. The proposition below shows that Q is a **false property** of N iff the truth tables T_{tbl} and T_{tbl}^* are incompatible i.e. $T_{tbl} \not\equiv T_{tbl}^*$. (If $T_{tbl} \Rightarrow T_{tbl}^*$ then T_{tbl}^* can be viewed just as a relaxation of T_{tbl} .)

Proposition 1: $F \not\equiv Q$ iff $T_{tbl} \not\equiv T_{tbl}^*$.

Proof: The “if” part. Let $T_{tbl} \not\equiv T_{tbl}^*$. Let (\bar{x}, \bar{z}) be an assignment to $X \cup Z$ such that $T_{tbl}(\bar{x}, \bar{z}) \not\equiv T_{tbl}^*(\bar{x}, \bar{z})$. (That is $T_{tbl}(\bar{x}, \bar{z}) = 1$ and $T_{tbl}^*(\bar{x}, \bar{z}) = 0$.) Let $\vec{p} = (\bar{x}, \vec{y}, \bar{z})$ be the assignment describing the execution trace in N under the input \bar{x} . Then \vec{p} satisfies F and hence F' . Assume the contrary, i.e. $F \Rightarrow Q$. Then $Q(\bar{x}, \bar{z}) = 1$. Since \vec{p} satisfies F' , then $Q \wedge \exists Y[F'] = \exists Y[G^* \wedge F'] = \exists Y[F^*] = T_{tbl}^* = 1$ under assignment (\bar{x}, \bar{z}) . So we have a contradiction.

The “only if” part. Let $F \not\equiv Q$. Let $\vec{p} = (\bar{x}, \vec{y}, \bar{z})$ be an assignment to $Vars(F)$ that satisfies F and falsifies Q (i.e. \vec{p} breaks $F \Rightarrow Q$). Since $F(\vec{p}) = 1$, then $T_{tbl}(\bar{x}, \bar{z}) = 1$. Since $Q(\bar{x}, \bar{z}) = 0$, then $Q \wedge \exists Y[F'] = \exists Y[G^* \wedge F'] = \exists Y[F^*] = T_{tbl}^* = 0$ under assignment (\bar{x}, \bar{z}) . So, $T_{tbl}(\bar{x}, \bar{z}) \not\equiv T_{tbl}^*(\bar{x}, \bar{z})$.

C. Test generation

Let $Q(X, Z)$ be a property of $N(X, Y, Z)$ obtained as described in the previous subsection. We are interested in tests that break Q . A single test of that kind can be extracted from an assignment $\vec{p} = (\bar{x}, \vec{y}, \bar{z})$ that satisfies F and falsifies Q thus breaking $F \Rightarrow Q$. Such an assignment \vec{p} can be found by running a SAT-solver on $F \wedge \bar{C}$ where C is a clause of Q . The \bar{x} part of \vec{p} is a *required test*.

Intuitively, tests breaking Q should be of high quality. The reason is that they are supposed to break a property that is “almost true”. Indeed, the proof of Proposition 1 shows that an assignment (\bar{x}, \bar{z}) breaking Q exposes the difference in the input/output behavior specified by F and F^* . The latter is not a trivial task assuming that F and F^* are almost identical. To substantiate our intuition, in the appendix, we show that stuck-at fault tests (that are tests of a very high quality) are a special case of tests breaking false properties.

³If this requirement does not hold, F^* may imply a non-empty set of clauses $Q(X)$. Since $F \not\equiv Q$, the formula Q is a trivial false property that just excludes some input assignments to X . (So any input falsifying Q is a counterexample.) In reality, the requirement in question can be *ignored* if one also ignores the spurious false properties $Q(X)$.

IV. A COMPLETE SET OF FALSE PROPERTIES

In the previous section, we introduced false properties as a means to deal with incompleteness of specification. In this section, we describe a procedure called *CmplSet* that constructs a set of false properties that is structurally complete. Here we borrow an idea exploited in testing: if functional completeness is infeasible, run tests probing every design piece to reach *structural* completeness. Similarly, structural completeness of a set of false properties is achieved by generating properties relating to different parts of the design.

A. Input/output parameters of the *CmplSet* procedure

In this section, we continue the notation of the previous section. The pseudocode of *CmplSet* is shown in Figure 1. It accepts five parameters: $\mathcal{P}^{hrd}, \mathcal{P}^{inf}, N, F, Y$. The parameter \mathcal{P}^{hrd} is the set of properties of specification $\mathcal{P} = \{P_1, \dots, P_k\}$ that were too hard to prove/disprove. The parameter \mathcal{P}^{inf} is an *informal* specification that is assumed to be *complete*⁴. The parameter N denotes a combinational circuit implementing the specification \mathcal{P} . The parameter F is a formula describing the functionality of N . Finally, the parameter Y is the set of internal variables of N .

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CmplSet( $\mathcal{P}^{hrd}, \mathcal{P}^{inf}, N, F, Y$ ) {
1   $\mathcal{T} := \emptyset$ 
2   $\mathcal{P}^{fls} := \emptyset$ 
3   $Gates := ExtrGates(N)$ 
4  while ( $Gates \neq \emptyset$ ) {
5     $g := PickGate(Gates)$ 
6     $Gates := Gates \setminus \{g\}$ 
7     $(G, G^*) := Change(F, g)$ 
8     $F' := F \setminus G$ 
9     $Q := PQE(G^*, F', Y)$ 
10    $Tst := RunSat(F, Q)$ 
11   if ( $Tst = nil$ ) continue
12    $\mathcal{P}^{fls} := \mathcal{P}^{fls} \cup \{Q\}$ 
13   if ( $BreaksProp(\mathcal{P}^{hrd}, Tst)$ )
14     return( $Tst, \mathcal{T}, \mathcal{P}^{fls}$ )
15   if ( $BreaksSpec(\mathcal{P}^{inf}, Tst)$ )
16     return( $Tst, \mathcal{T}, \mathcal{P}^{fls}$ )
17    $\mathcal{T} := \mathcal{T} \cup \{Tst\}$ 
18 return( $nil, \mathcal{T}, \mathcal{P}^{fls}$ )

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Fig. 1. The *CmplSet* procedure

CmplSet has three output parameters: $Tst, \mathcal{T}, \mathcal{P}^{fls}$. The parameter Tst denotes a test exposing a bug of N (if any). The parameter \mathcal{T} consists of tests generated by *CmplSet* that has identified any bug. (These tests may still be of value e.g. for regression testing). The parameter \mathcal{P}^{fls} denotes the set of false properties generated by *CmplSet*.

B. The while loop of the *CmplSet* procedure

The main body of *CmplSet* consists of a while loop (lines 4-17). This loop is controlled by the set $Gates$ consisting of gates of N . Originally, $Gates$ is set to the set of all gates of N (line 3). *CmplSet* starts an iteration of the loop by extracting a

⁴One can view \mathcal{P}^{inf} as a replacement for the truth table. The role of such a replacement can be played, for instance, by the designer.

gate g of *Gates* (lines 5-6). Then *CmplSet* computes formula G^* that replaces the clauses of G (describing the gate g) in formula F (line 7). After that, *CmplSet* calls a PQE solver to find a formula $Q(X, Z)$ such that $\exists Y[G^* \wedge F'] \equiv Q \wedge \exists Y[F']$ where $F' = F \setminus G$. The formula Q above represents a property of N that is supposed to be false⁵.

CmplSet checks if Q is indeed a false property by running a SAT-solver that looks for an assignment breaking $F \Rightarrow Q$ (line 10). If this SAT-solver fails to find such an assignment, Q is a true property. In this case, *CmplSet* starts a new iteration (line 11). Otherwise, the SAT-solver returns a test Tst and Q is added to \mathcal{P}^{fls} as a new false property. Then *CmplSet* checks if Tst breaks an unproved property of \mathcal{P}^{hrd} . If it does, then *CmplSet* terminates (lines 13-14). After that, *CmplSet* checks if Tst violates the informal specification \mathcal{P}^{inf} . If so, then *CmplSet* terminates (line 15-16). Finally, *CmplSet* adds Tst to \mathcal{T} and starts a new iteration.

V. EXTENSION TO SEQUENTIAL CIRCUITS

In this section, we extend our approach to sequential circuits. Subsection V-A provides some relevant definitions. In Subsection V-B, we give a high-level view of building a structurally complete set of false properties for a sequential circuit (in terms of safety properties). Finally, Subsection V-C describes generation of false safety properties.

A. Some relevant definitions

Let $M(S, X, Y, S')$ be a sequential circuit. Here X, Y denote input and internal combinational variables respectively and S, S' denote the present and next state variables respectively. Let $F(S, X, Y, S')$ be a formula describing the circuit M . (F is built for M in the same manner as for a combinational circuit N , see Section II.) Let $I(S)$ be a formula specifying the *initial states* of M . Let $T(S, S')$ denote $\exists X \exists Y[F]$ i.e. the *transition relation* of M .

A *state* \vec{s} is an assignment to S . Any formula $P(S)$ is called a *safety property* for M . A state \vec{s} is called a *P-state* if $P(\vec{s}) = 1$. A state \vec{s} is called *reachable in n transitions* (or in *n -th time frame*) if there is a sequence of states $\vec{s}_1, \dots, \vec{s}_{n+1}$ such that \vec{s}_1 is an I -state, $T(\vec{s}_i, \vec{s}_{i+1}) = 1$ for $i = 1, \dots, n$ and $\vec{s}_{n+1} = \vec{s}$.

We will denote the *reachability diameter* of M with initial states I as $Diam(M, I)$. That is if $n = Diam(M, I)$, every state of M is reachable from I -states in at most n transitions. We will denote as $\mathbf{Rich}(M, I, n)$ a formula specifying the set of states of M reachable from I -states in n transitions. We will denote as $\mathbf{Rich}(M, I)$ a formula specifying all states of M reachable from I -states. A property P *holds* for M with initial states I , if no \overline{P} -state is reachable from an I -state. Otherwise, there is a sequence of states called a *counterexample* that reaches a \overline{P} -state.

⁵Note that any subset of clauses of Q is a property as well. So, to decrease the complexity of PQE-solving, one can stop it when a threshold number of clauses is generated. Moreover, from the viewpoint of test generation, one can stop PQE *as soon as* a clause $C(X, Z)$ not implied by F is generated.

B. High-level view

In this paper, we consider a specification of the sequential circuit M above in terms of safety properties. So, when we say a specification property $P(S)$ of M we mean a *safety property*. Let $F_{1,n}$ denote $F_1 \wedge \dots \wedge F_n$ where F_i , $1 \leq i \leq n$ is the formula F in i -th time frame i.e. expressed in terms of sets of variables S_i, X_i, Y_i, S_{i+1} . Formula $Rch(M, I, n)$ can be computed by QE on formula $\exists W_{1,n}[I_1 \wedge F_{1,n}]$. Here $I_1 = I(S_1)$ and $W_{1,n} = Vars(F_{1,n}) \setminus S_{n+1}$. If $n \geq Diam(M, I)$, then $Rch(M, I, n)$ is also $Rch(M, I)$ specifying all states of M reachable from I -states.

Let $\mathcal{P} = \{P_1, \dots, P_k\}$ be a set of properties forming a *specification* of a sequential circuit with initial states defined by I . Let a sequential circuit M be an implementation of the specification \mathcal{P} . So every property $P_i, i = 1, \dots, k$ holds for M and I i.e. $Rch(M, I) \Rightarrow P_i, i = 1, \dots, k$. Verifying the completeness of \mathcal{P} reduces to checking if $P_1 \wedge \dots \wedge P_k \Rightarrow Rch(M, I)$. Assume that proving this implication is hard or it does not hold. If \mathcal{P} is incomplete, M may be buggy for two reasons mentioned in the introduction. In particular, M may falsify a property absent from \mathcal{P} . (This means that there is a reachable state \vec{s} of M that satisfies all properties of \mathcal{P} and \vec{s} is supposed to be unreachable.)

One can deal with the problem above like it was done in the case of combinational circuits. Namely, one can use PQE to build false properties that are supposed to imitate properties that the specification \mathcal{P} has missed. By building counterexamples one generates “interesting” reachable states. If one of these reachable states is supposed to be *unreachable*, M has a bug.

C. Generation of false properties

False properties of a sequential circuit $M(S, X, Y, S')$ can be generated as follows. Recall that formula $\exists W_{1,n}[I_1 \wedge F_{1,n}]$ specifies $Rch(M, I, n)$ (see the previous subsection). Here $I_1 = I(S_1)$ and $W_{1,n} = Vars(F_{1,n}) \setminus S_{n+1}$. Let G be a (small) subset of clauses of $F_{1,n}$. Let G^* be a set of clauses meant to replace G . We assume that G^* satisfies two requirements similar to those mentioned in Subsection III-B. (In particular, we impose an informal requirement that G^* is unlikely to be implied by $I_1 \wedge F_{1,n}$.)

Let $Q(S_{n+1})$ be a solution to the problem of taking G^* out of the scope of quantifiers in $\exists W_{1,n}[I_1 \wedge G^* \wedge F'_{1,n}]$ where $F'_{1,n} = F_{1,n} \setminus G$. That is $\exists W_{1,n}[I_1 \wedge G^* \wedge F'_{1,n}] \equiv Q \wedge \exists W_{1,n}[I_1 \wedge F'_{1,n}]$. By definition, Q is a property M (as a predicate depending only on variables of S). To show that Q is a *false* property one needs to find an assignment breaking $I_1 \wedge F_{1,n} \Rightarrow Q$. If such an assignment exists, there is a counterexample proving that a \overline{Q} -state is reachable in n transitions. In this case, Q is indeed a false property.

Using the idea above and a procedure similar to that of Section IV, one can build a structurally complete set of false safety properties.

VI. OUR APPROACH AND FAULT/MUTATION DETECTION

Generation of tests breaking false properties is similar to fault/mutation detection. In manufacturing testing, one generates tests detecting faults of a predefined set [1], [4]. Often, these faults (e.g. stuck-at faults) do not simulate real defects but rather model logical errors. In software verification, one of old techniques gaining its popularity is mutation testing [3], [2]. The idea here is to introduce code mutations (e.g. simulating common programmer mistakes) to check the quality of an existing test suite or to generate new tests.

Our approach has three potential advantages. First, PQE solving introduces a new way to generate tests detecting faults/mutations. (In the appendix, we give an example of using PQE for stuck-at fault testing.) The appeal of PQE here is that it can take into account subtle structural properties like unobservability. So PQE-solvers can potentially have better scalability than tools based purely on identifying logical inconsistencies (also known as conflicts).

The second advantage of our approach is that it transforms a fault/mutation into a property i.e. into a *semantic* notion. This has numerous benefits. One of them is that a false property specifies a large number of tests (rather than a single test). Suppose, for instance, that we need to find a single test detecting faults ϕ_1 and ϕ_2 of a circuit. An obvious problem here is that a test detecting one fault may not detect the other. In our approach, ϕ_1 and ϕ_2 are cast as false properties Q_1 and Q_2 . To break Q_1 or Q_2 one needs to come up with a test satisfying $\overline{Q_1}$ or $\overline{Q_2}$. To break *both* properties one just needs to find a test satisfying $\overline{Q_1} \wedge \overline{Q_2}$ (if any).

Third, our approach can be applied to *abstract* formulas that may not even describe circuits or programs. So, in a sense, the machinery of false properties can be viewed as a generalization of fault/mutation detection.

VII. CONCLUSIONS

Having an incomplete specification may lead to a buggy implementation. One of the problems here is that this implementation may not satisfy a property omitted in the specification. We address this problem by generating false properties i.e. those that are not consistent with the implementation. The idea here is that a test breaking a false property may also expose a bug in the implementation. False properties are generated by a technique called partial quantifier elimination (PQE).

Our three conclusions are as follows. First, the machinery of false properties can be applied to verification of combinational and sequential circuits. The efficiency of this machinery depends on that of PQE solving. So developing powerful PQE algorithms is of great importance. Second, the machinery of false properties can be viewed as a generalization of fault/mutation detection. On one hand, this implies that tests breaking false properties are of high quality. On the other hand, this means that the machinery of false properties can be applied to abstract formulas. Third, by generating properties whose falsehood is caused by different parts of the design, one generates a “structurally complete” set of false properties.

Using tests that break all properties of this set can significantly increase the quality of testing.

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APPENDIX

STUCK-AT FAULT TESTS AND FALSE PROPERTIES

In this appendix, we relate stuck-at faults tests and those breaking false properties built by PQE. This relation suggests that tests breaking false properties are of high quality. Subsection A briefly recalls stuck-at fault testing. In Subsection B, we consider a special case of Proposition 1 where a false property is generated by modifying the original circuit to *another circuit*. Subsection C describes how stuck-at faults are modeled in our approach. Finally, in Subsection D, we discuss generation of stuck-at fault tests by PQE.

A. Recalling stuck-at fault testing

A stuck-at fault is an abstract model of a fault in a combinational circuit where a line is stuck either at value 0 (stuck-at-0 fault) or 1 (stuck-at-1 fault). In current technology, a stuck-at fault does not simulate an actual defect but rather serves as a *logical* fault model. Tests detecting stuck-at faults are typically used in manufacturing testing. However, they can also be employed in design verification. The appeal of the stuck-at model is in the high-quality of tests detecting stuck-at faults. It can be attributed to probing corner input/output behaviors by these tests.

B. A special case of false properties built by PQE

In this section, we continue the notation of Section III. Let $N(X, Y, Z)$ be a combinational circuit and $F(X, Y, Z)$ be a formula specifying N . Let G be a subset of clauses of F . Then formula F can be represented as $G \wedge F'$ where $F' = F \setminus G$. Let F^* be a formula obtained from F by replacing G with a set of clauses G^* i.e. $F^* = G^* \wedge F'$.

In Subsection III-B, we considered generation of property $Q(X, Z)$ by taking G^* out of the scope of quantifiers in $\exists Y[G^* \wedge F']$. There, we imposed the requirement that for every assignment \vec{x} there was \vec{z} such that $T_{tbl}^*(\vec{x}, \vec{z})=1$ where $T_{tbl}^* = \exists Y[F^*]$. In this section, we strengthen this requirement by claiming that for every \vec{x} there exists exactly one \vec{z} such that $T_{tbl}^*(\vec{x}, \vec{z})=1$. Then one can formulate a stronger version of Proposition 1 (recall that T_{tbl} denotes $\exists Y[F]$).

Proposition 2: $F \not\equiv Q$ iff $T_{tbl} \not\equiv T_{tbl}^*$.

Proof: Since we consider a special case, Proposition 1 holds and so $F \not\equiv Q$ iff $T_{tbl} \not\equiv T_{tbl}^*$. Let us show that under the new requirement to T_{tbl}^* above, $T_{tbl} \Rightarrow T_{tbl}^*$ entails $T_{tbl} \equiv T_{tbl}^*$. (Since $T_{tbl} \equiv T_{tbl}^*$ trivially implies $T_{tbl} \Rightarrow T_{tbl}^*$, this means that $T_{tbl} \not\equiv T_{tbl}^*$ entails $T_{tbl} \not\Rightarrow T_{tbl}^*$.) Assume the contrary i.e. $T_{tbl} \not\equiv T_{tbl}^*$. The only possibility here is that there exists an assignment (\vec{x}, \vec{z}) to $X \cup Z$ such that $T_{tbl}(\vec{x}, \vec{z}) = 0$ and $T_{tbl}^*(\vec{x}, \vec{z}) = 1$. Let \vec{z}' be the output produced by circuit N for the input \vec{x} . Then $T_{tbl}(\vec{x}, \vec{z}')=1$. Since $T_{tbl} \Rightarrow T_{tbl}^*$ then $T_{tbl}^*(\vec{x}, \vec{z}')=1$ too. But this violates the strengthened requirement on T_{tbl}^* because $T_{tbl}^*(\vec{x}, \vec{z})$ and $T_{tbl}^*(\vec{x}, \vec{z}')$ are equal to 1 for the same \vec{x} .

Remark 2: The strengthened requirement imposed on T_{tbl}^* holds if, for instance, F^* specifies a circuit N^* obtained by a modification of N . Proposition 2 implies that a test breaking the property Q also makes N and N^* produce different outputs and vice versa. So, if N^* describes a faulty version of N , a test breaking Q detects this fault and vice versa.

C. An example of modeling a stuck-at fault

Let g be a gate of circuit N given in Example 1. That is g is a 2-input AND gate specified by $v_3 = v_1 \wedge v_2$. The functionality of g is described by $C_1 \wedge C_2 \wedge C_3$ where $C_1 = v_1 \vee \bar{v}_3$, $C_2 = v_2 \vee \bar{v}_3$, $C_3 = \bar{v}_1 \vee \bar{v}_2 \vee v_3$. Here C_1, C_2, C_3 are clauses of the formula F specifying N .

Let N^* denote the circuit obtained from N by introducing the stuck-at-0 fault at the output of g . A formula F^* specifying N^* is obtained from F by replacing C_3 with the clause $C_3^* = \bar{v}_1 \vee \bar{v}_2 \vee \bar{v}_3$. (It is not hard to check that by resolving clauses C_1, C_2 and C_3^* on v_1 and v_2 one obtains the clause \bar{v}_3 .) So $F^* = C_3^* \wedge F'$ where $F' = F \setminus \{C_3\}$. By taking C_3^* out of the scope of quantifiers in $F^* = C_3^* \wedge F'$ one obtains a property $Q(X, Z)$. That is $\exists Y[C_3^* \wedge F'] \equiv Q \wedge \exists Y[F']$. Assume that Q is a false property i.e. there exists an assignment $\vec{p}=(\vec{x}, \vec{y}, \vec{z})$ breaking $F \Rightarrow Q$. Then \vec{x} makes N and N^* produce different outputs i.e. \vec{x} is a *test* detecting the stuck-at fault at hand.

D. Finding stuck-at fault tests by PQE

If one needs to find a single test detecting a stuck at-fault, there is no need to generate the entire false property Q above. For instance, in the previous subsection, one can stop taking C_3^* out of the scope quantifiers, as soon as a clause $B(X, Z)$ not implied by F is generated. Then a test can be extracted from an assignment satisfying $F \wedge \bar{B}$ (i.e. breaking $F \Rightarrow B$). So, PQE can be used for generation of fault-detecting tests.

Modern tools for generation of fault detecting tests are a combination of dedicated ATPG methods pioneered by the D-algorithm [11] and SAT-based algorithms [9], [10]. To make

a generic SAT-solver work in the ATPG setting, some extra work is done. For instance, extra variables and clauses are added to simulate signal propagation [8]. The appeal of ATPG by PQE-solving is that the latter takes the best of both worlds. On one hand, like a SAT-solver with conflict clause learning, a PQE-algorithm employs powerful methods of learning [6]. (In reality, the learning of a PQE-solver is more powerful since in addition to deriving conflict clauses, a PQE-solver also learns *non-conflict clauses*.) On the other hand, the machinery of clause redundancy [7], can take into account some subtle structural properties of the circuit at hand (e.g. observability). In particular, the redundancy based reasoning of a PQE-solver makes simulating signal propagation quite effortless and does not require adding new variables and clauses.